**Digital Systems**

**Principles and Applications**

|  |  |
| --- | --- |
| **SL No.** | **Content** |
| **01** | **Digital Number System.** |
| **02** | **Logic Gates and Boolean Algebra.** |
| **03** | **Addition operation , Combinational logic circuit [Half,Full (Adder, Subtractor)].** |
| **04** | **Code Conversion (Decimal-BCD-EX 3), 4 bit full adder, Carry propagation(Look ahead carry generator).** |
| **05** | **BCD Adder-Decimal Adder (4 bit parallel adder),** Magnitude Comparator. |
| **06** | Explaination of magnitude comparator (4 bit magnitude comparator); Homework: 8 bit mag. Comp. |
| **07** | **Encoder,** **Priority encoder**, **Decoder, Mux**, 1 bit full adder. |
| **08** | **DEMUX, subtractor(using k map),** **parallel subtractor.** |
| **09** | Memory design, Memory devices, General memory operation, Write operation, Rom, 16x8 ROM fig, ROM'S block diagram and explaination, 16x8 ROM internal architecture; (\*\*\*Figure 12.3 for 10 marks, Fig 12.5, Example 12.2). |
| **10** | Types of ROM's, block diagram, advantages & disadvantages, PROM, EPROM, EEPROM read & write operation. |
| **11** | Embedded microcontroller program memory, bootstrap memory, semiconductor RAM, \*RAM Architecture(Read, Write), Static RAM, Static RAM timing diagram(Read, Write), DRAM(advantages, disadvantages). |
| **12** | PLD, ROM as PLD, PLA. |
| **13** | PAL, Implementation of logic circuit using PAL, Truth table or ckt diagram(as a question for PAL), Slide page 14 of PAL. |
| **14** | Processor unit employing a scratchpad memory, design arithmatic ckt, logic diagram of arithmatic ckt, design of logic circuit(one stage), combining logic and arithmatic ckts, logic diagram of ALU; self study: 4 bit adder/subtractor ckt. |
| **15** | \*\*\*Chapter 9: Processor Logic Design (1 Set). |